I Claim:

1. A memory cell for permanently storing data, comprising:

a memory material capable of assuming a first, high-resistance state and a second, low-resistance state;

a heating device configured to heat said memory material at different heating rates to a programming temperature, said memory material having a relatively high resistance or a relatively low resistance after cooling, depending on the heating rate;

said heating device having a switching device and a heating element in direct proximity with said memory material, and said switching device having a field-effect transistor with a drain region formed as a heating region.

2. The memory cell according to claim 1, wherein said drain region comprises a highly doped contact-making region for making contact with said memory material.

3. The memory cell according to claim 1, wherein said field-effect transistor is formed vertically in a substrate, and an insulation material having low thermal conductivity surrounds said field effect transistor.

4. The memory cell according to claim 3, wherein said insulation material contains a silicon compound.

5. The method cell according to claim 4, wherein said insulation material is a silicon compound selected from the group consisting of silicon dioxide and silicon nitride.

6. A memory cell for permanently storing data, comprising:

a memory material capable of assuming a first, high-resistance state and a second, low-resistance state;

a heating device configured to heat said memory material at different heating rates to a programming temperature, said memory material having a relatively high resistance or a relatively low resistance after cooling, depending on the heating rate;

said heating device having a switching device and a heating element in direct proximity with said memory material, and said heating element has a diode device.

7. The memory cell according to claim 6, wherein said diode device is a diode or a diode chain.

8. The memory cell according to claim 6, wherein said diode device is formed by a semiconductor material exhibiting functionality at a programming temperature.

9. The memory cell according to claim 6, wherein said switching device is a transistor.

10. The memory cell according to claim 6, wherein said switching device is a field-effect transistor or a bipolar transistor.

11. The memory cell according to claim 6, wherein said switching device has a field-effect transistor and said diode device is formed by a layer sequence on a drain region of said field-effect transistor.

12. The memory cell according to claim 11, which comprises a thermal resistor formed between said layer sequence of said diode device and said drain region of said field-effect transistor.

13. The memory cell according to claim 12, wherein said thermal resistor is a highly conductive semiconductor layer.

14. The memory cell according to claim 6, wherein said thermal resistor is a highly doped semiconductor layer.

15. The memory cell according to claim 6, wherein said diode device comprises one of more Zener diodes.